A Si-Compatible Fabrication Process for Scaled Self-Aligned InGaAs FinFETs

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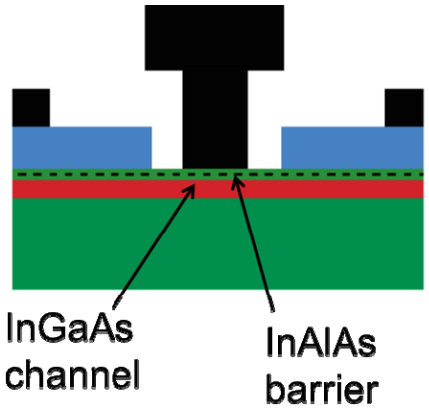
Lam Research

Outline

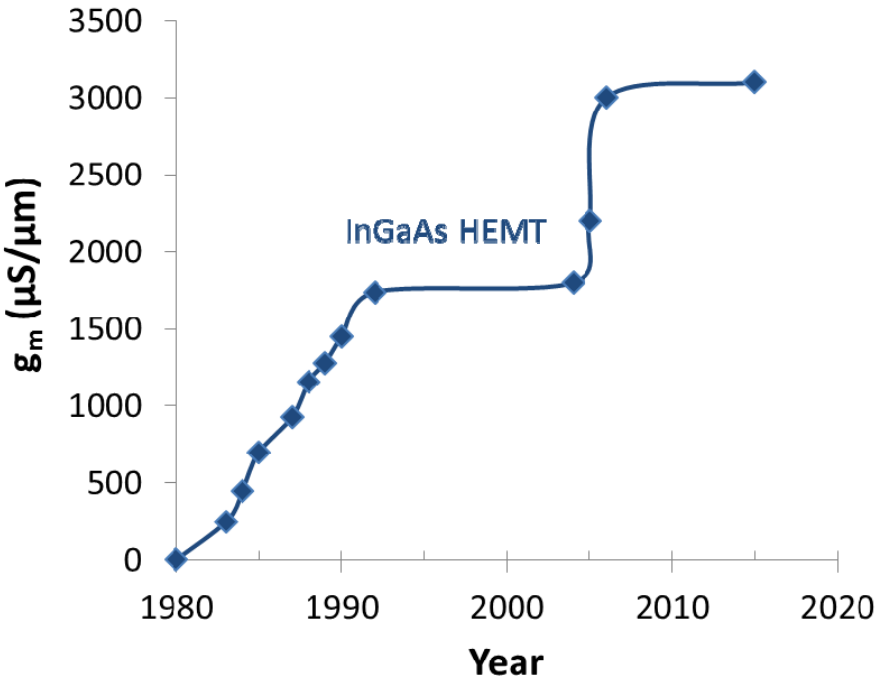
- Motivation
- Process technology
- Electrical characteristics
- Late news
- Conclusions

Historical evolution: InGaAs High-Electron Mobility Transistor

High-Electron Mobility Transistor



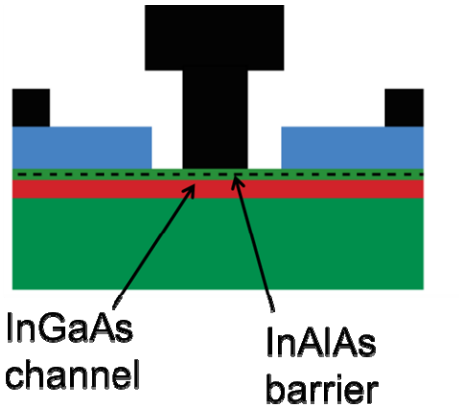
Transconductance ($g_m=dI_D/dV_{GS}$):



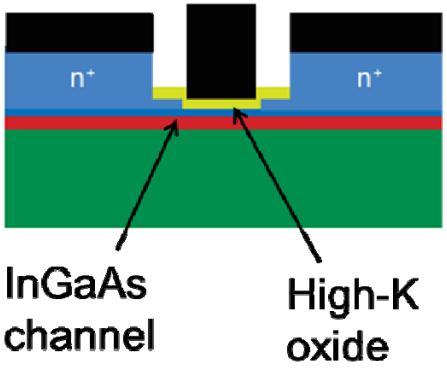
- Superior electron transport properties in InGaAs

InGaAs MOSFETs vs. HEMTs

High-Electron Mobility Transistor



Metal-Oxide-Semiconductor
Field-Effect Transistor



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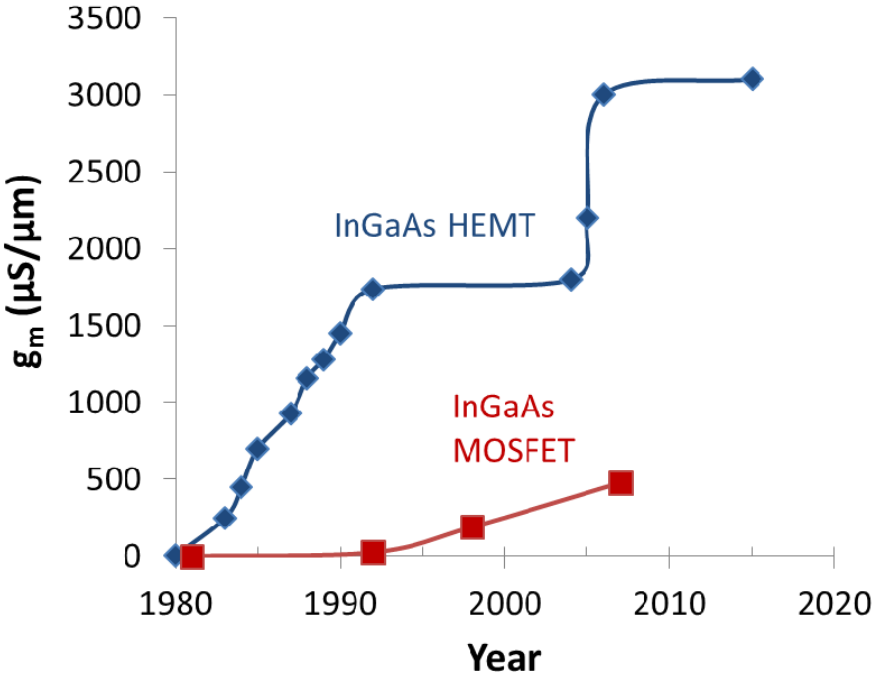
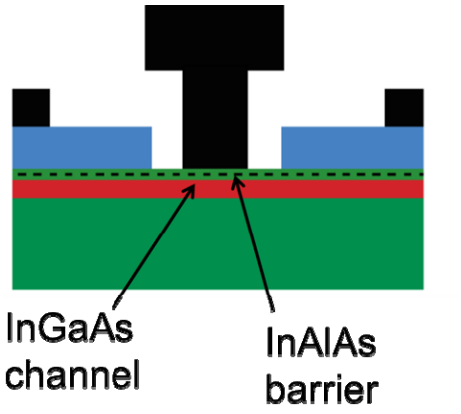


- Superior electron transport properties in InGaAs

InGaAs MOSFETs vs. HEMTs

High-Electron Mobility Transistor



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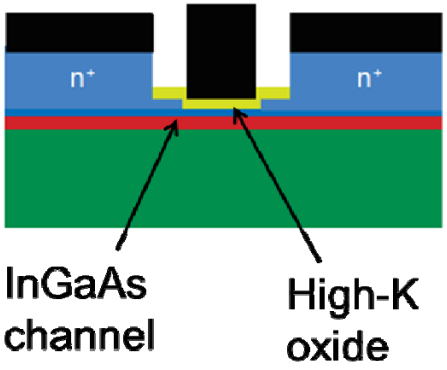

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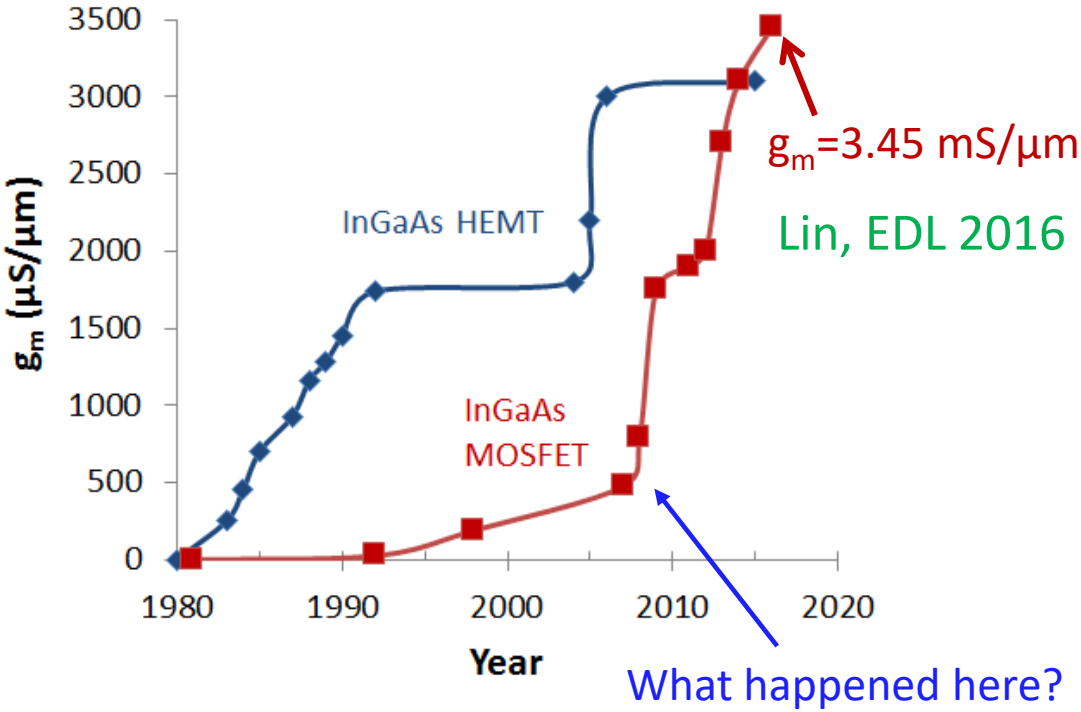
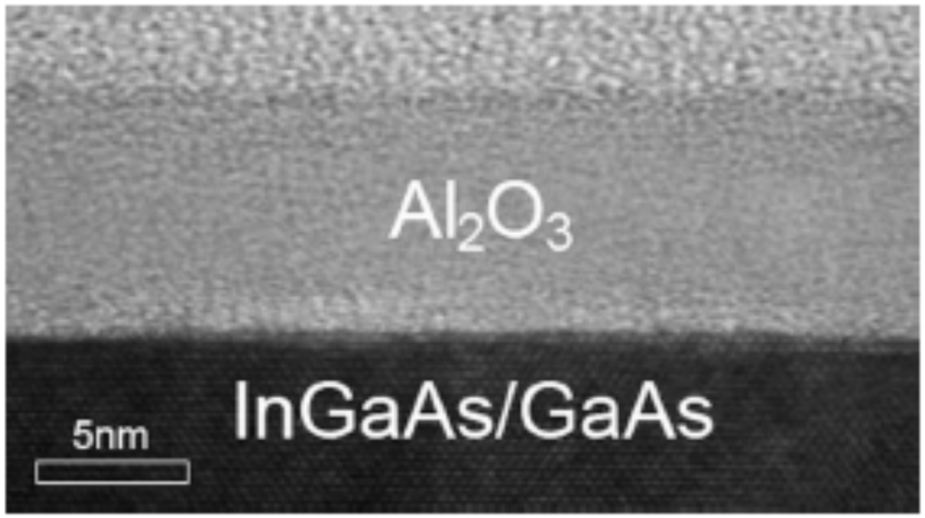


- Superior electron transport properties in InGaAs
- InGaAs planar MOSFET performance exceeds that of High Electron Mobility Transistors (HEMT)

Atomic Layer Deposition (ALD) of gate oxide

ALD eliminates residual native oxides that pin Fermi level

→ "Self cleaning"

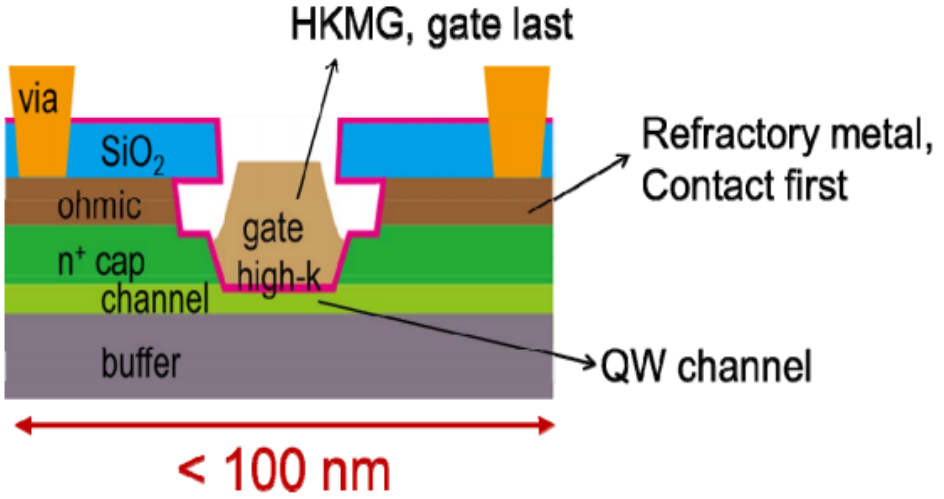


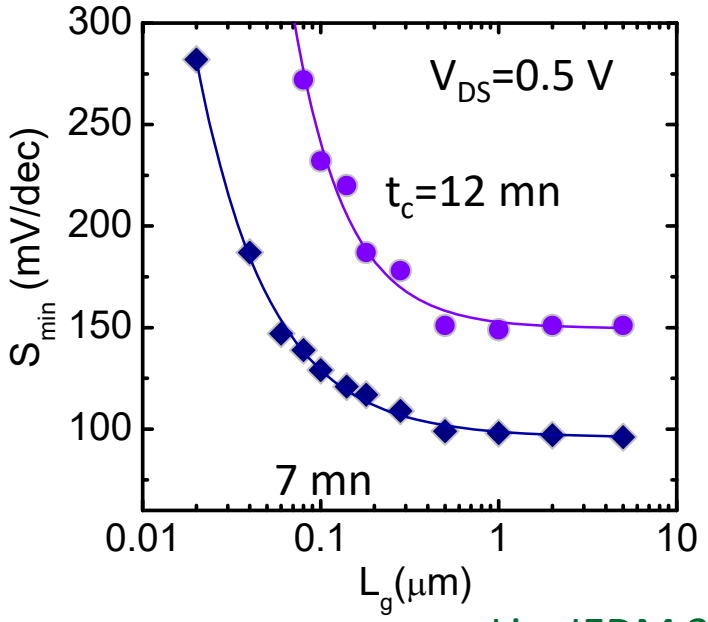
Huang, APL 2005

← Clean, smooth interface without native oxides

- First with Al_2O_3, then with other high-K dielectrics
- First in GaAs, then in other III-Vs

InGaAs planar Quantum-Well MOSFETs - short-channel effects

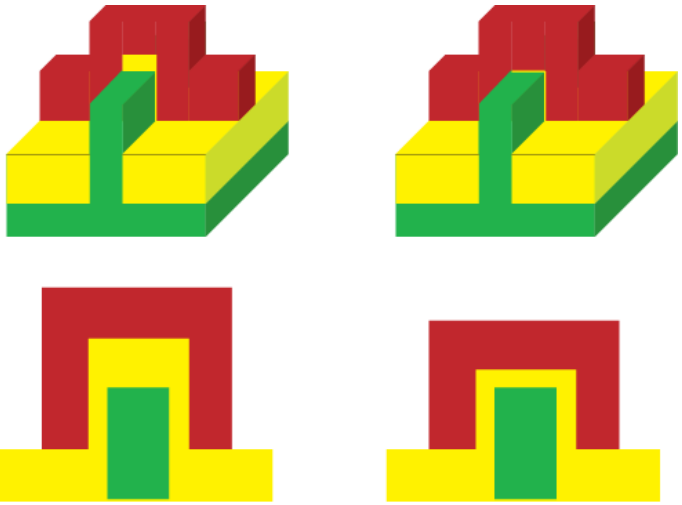




Lin, IEDM 2014

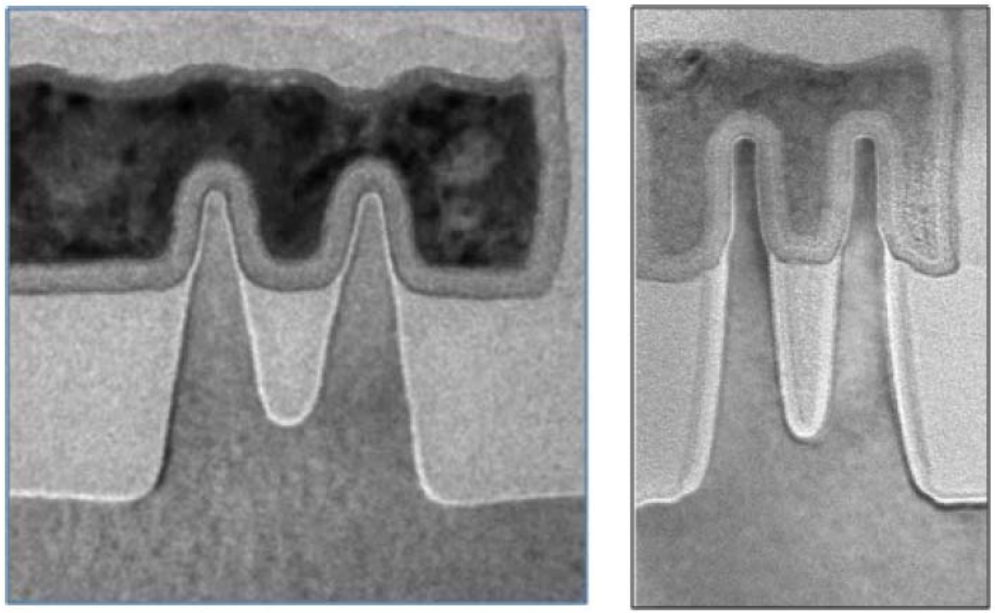
- Short-channel effects limit scaling to L_g~40 nm
- 3D transistors required for further scaling

FinFETs



Double-gate MOSFET Tri-gate MOSFET

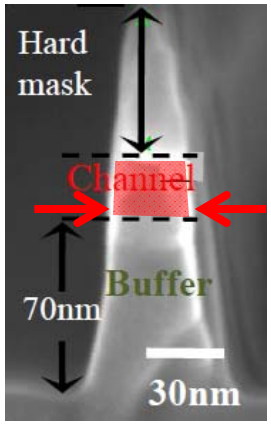
Intel Si Trigate MOSFETs



22 nm Process 14 nm Process

- FinFETs used in state-of-the-art Si CMOS
- Good balance of SCE and high ON current per footprint

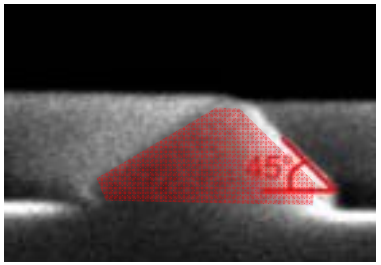
InGaAs FinFETs



W_f~30 nm

Thathachary, VLSI 2015

W_f~25 nm

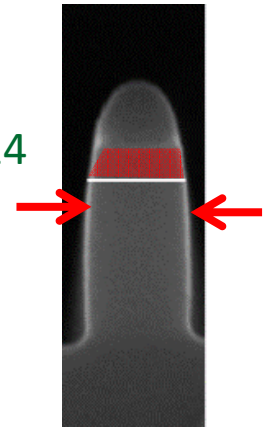


Zota, IEDM 2016

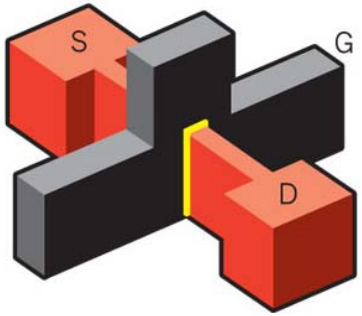
W_f~50 nm

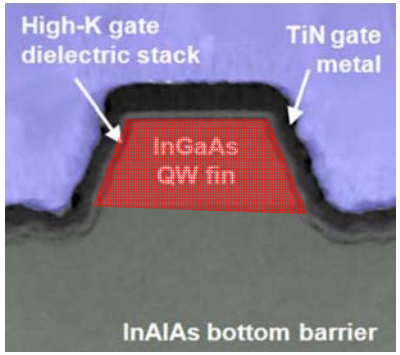
Waldron, VLSI 2014

W_f~50 nm

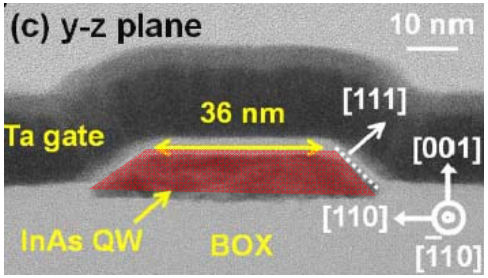


Kim, IEDM 2013



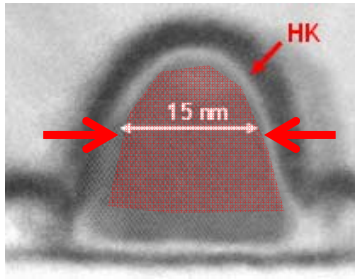


Radosavljevic ,IEDM 2011



Kim, TED 2014

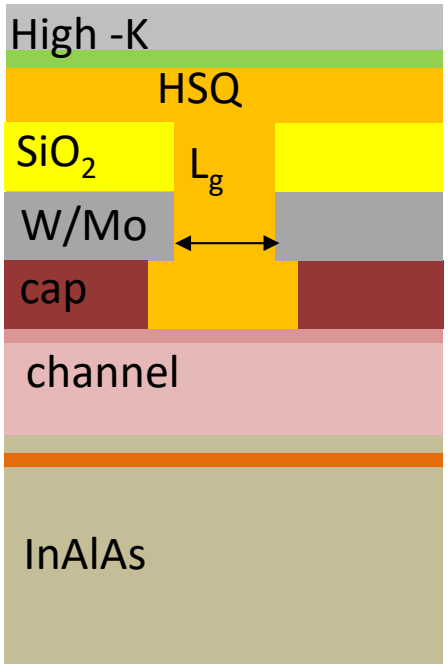
W_f~15 nm

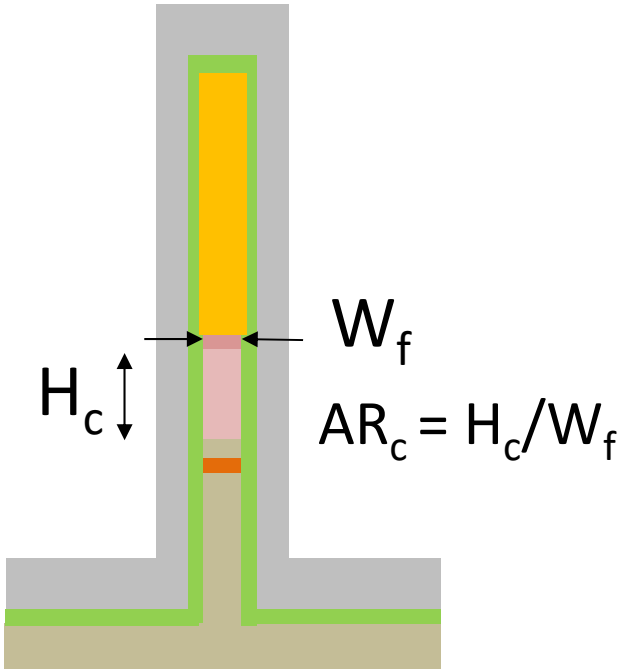


Djara, VLSI 2015

- Demonstrations to date: $W_f \geq 15$ nm, $AR_c \leq 2$

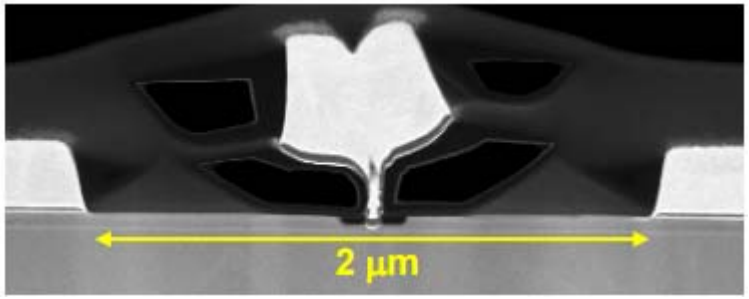
Goal: Sub-10 nm W_f Self-aligned III-V FinFETs





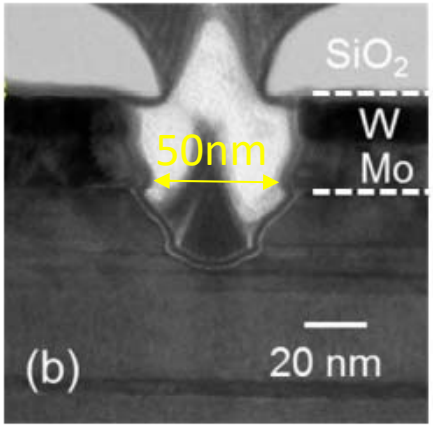
- Deeply scaled W_f, L_g and EOT
- High channel aspect ratio (AR_c)
- Self-aligned contacts
- CMOS-compatible processes and materials in front-end

From InGaAs HEMT to finFET



InGaAs HEMT

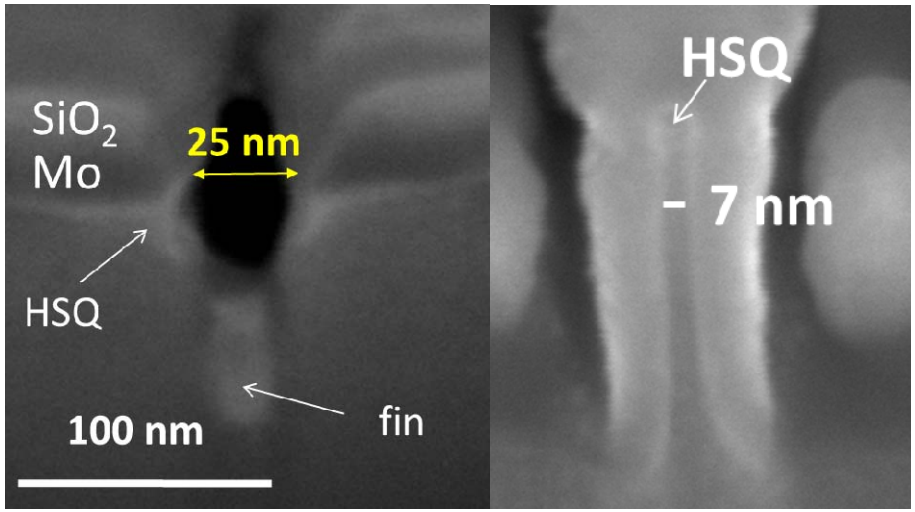
del Alamo, CS MANTECH 2011



InGaAs Planar MOSFET

Lin, CS MANTECH 2015

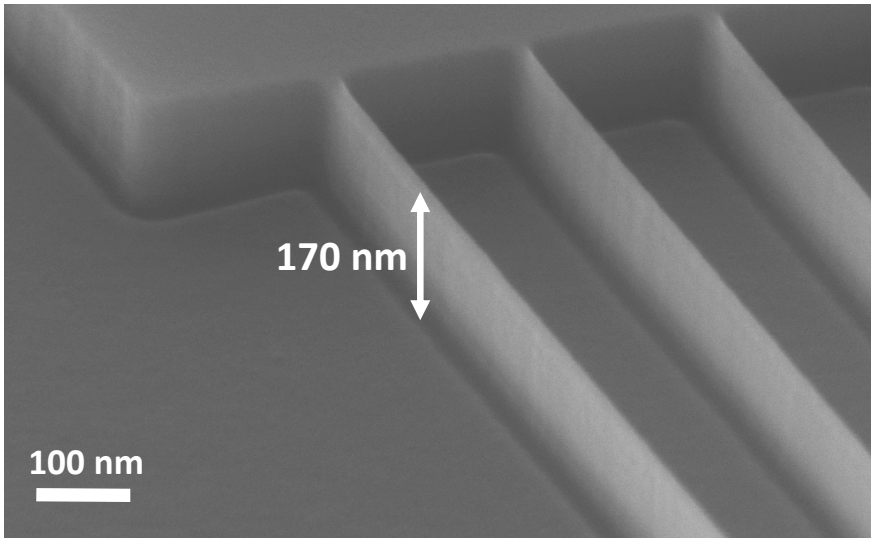
- Contact first
- Gate recess

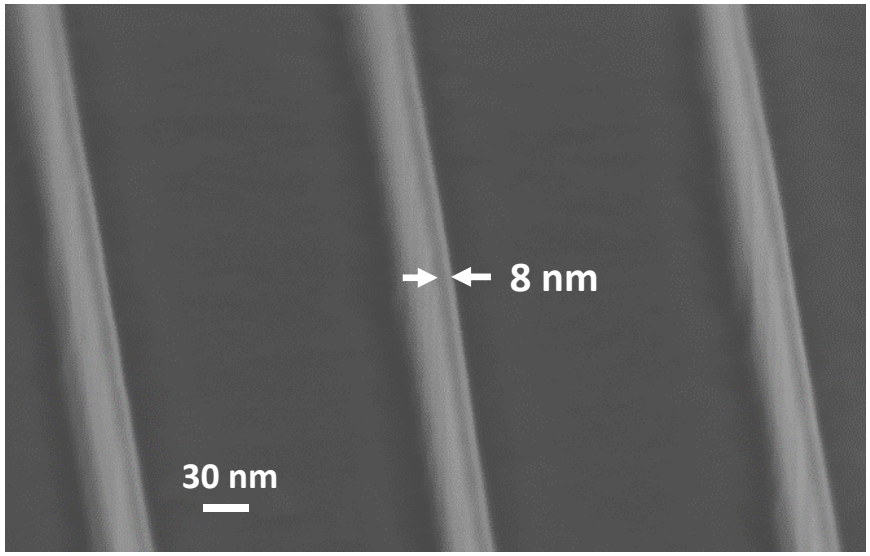


InGaAs FinFET

Vardi, CSMANTECH 2017

Fin definition:
RIE + Digital etch

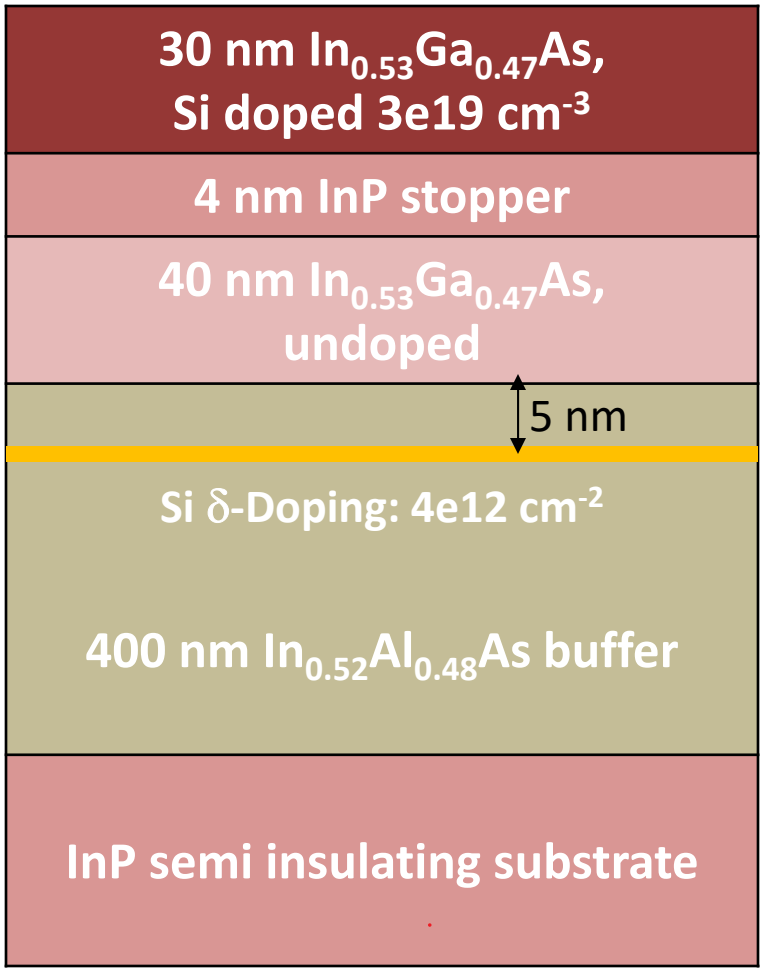




- **$BCl_3/SiCl_4$/Ar RIE:**
  smooth, vertical sidewalls and high aspect ratio (>10)
- **Digital etch (DE)**:
  self-limiting O_2 plasma oxidation + H_2SO_4 oxide removal

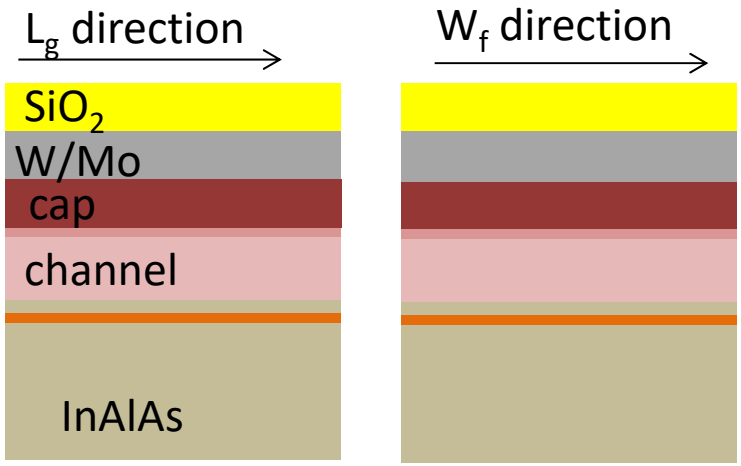
Zhao, EDL 2014
Vardi, VLSI 2016

Device fabrication



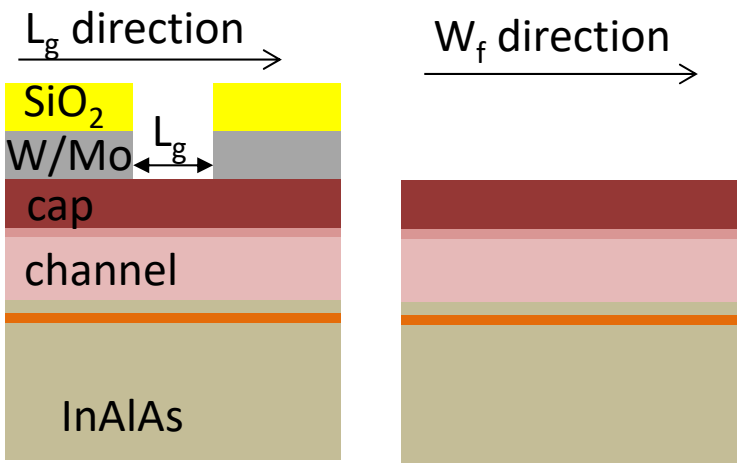
- Highly doped cap
- 40 nm thick channel layer
- Delta doping underneath

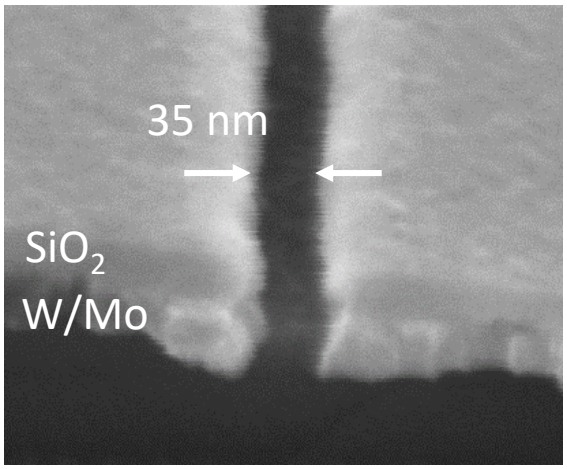
Device fabrication



- Sputtered W/Mo contact
- CVD SiO_2 hard mask

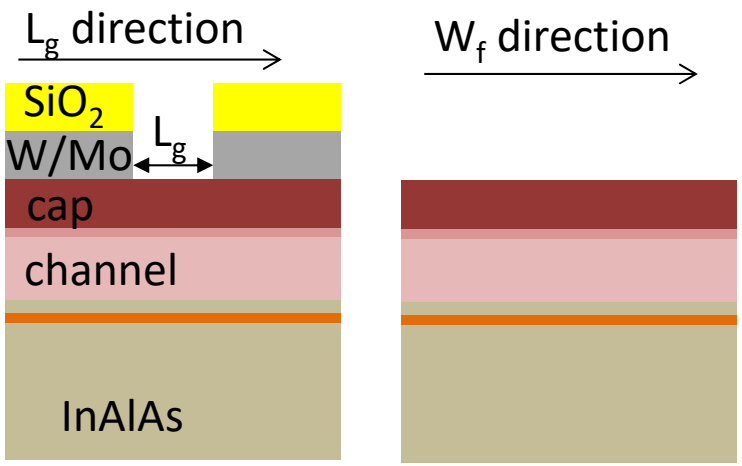
Device fabrication

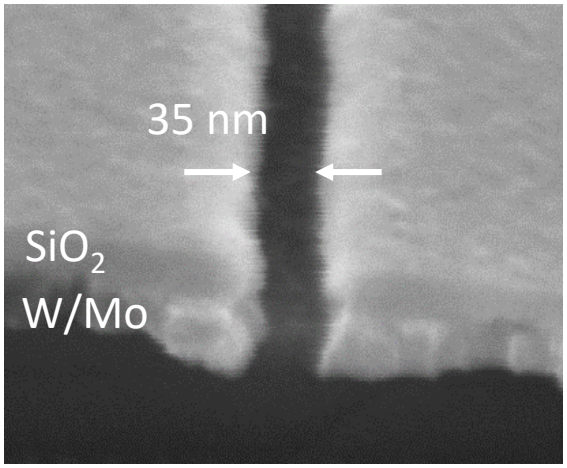




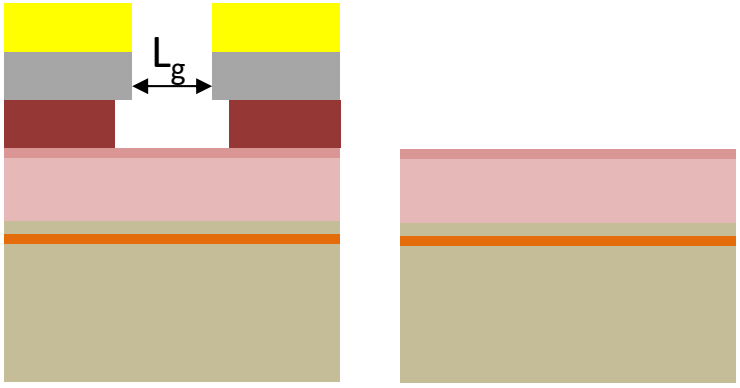
- Sputtered W/Mo contact
- CVD SiO_2 hard mask
- Gate lithography
- Gate recess (Dry): SiO_2/W/Mo
- Active area definition

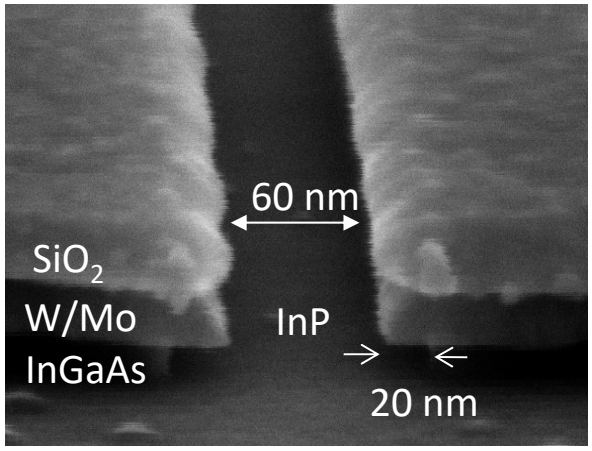
Device fabrication



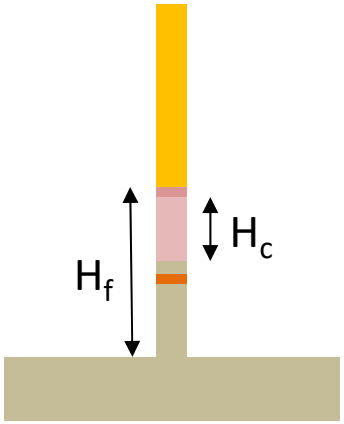


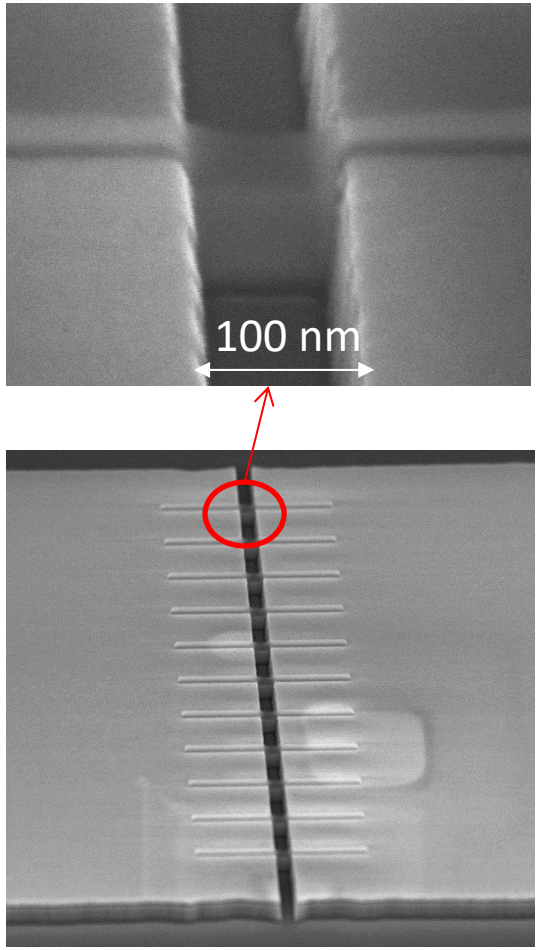
- Sputtered W/Mo contact
- CVD SiO_2 hard mask
- Gate lithography
- Gate recess (Dry): SiO_2/W/Mo
- Active area definition
- Gate recess (Wet): Cap etch





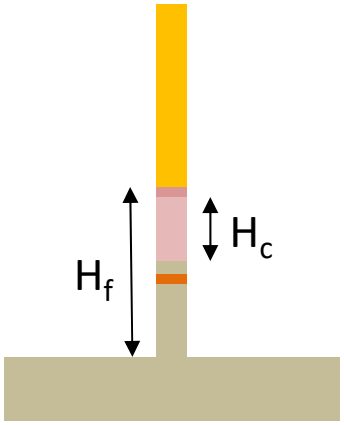
Device fabrication

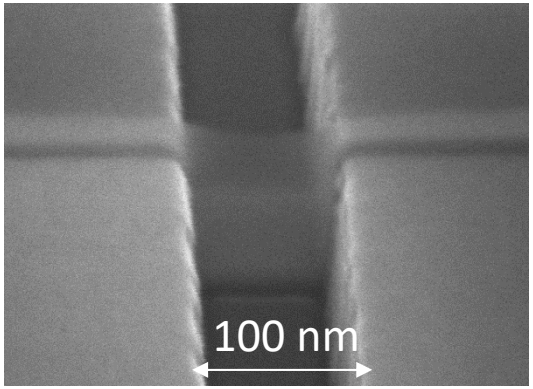




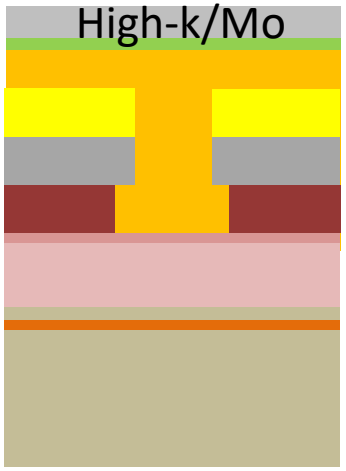
- Sputtered Mo contact
- CVD SiO_2 hard mask
- Gate lithography
- Gate recess (Dry): SiO_2/W/Mo
- Active area definition
- Gate recess (Wet): Cap etch
- Fin Lithography
- Fin etch

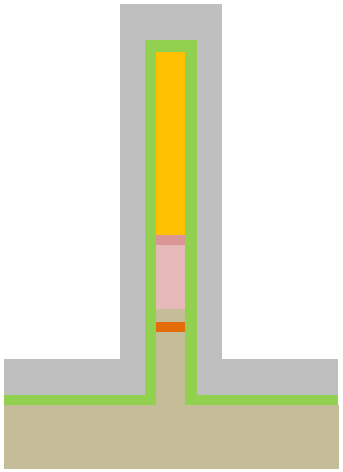
Device fabrication

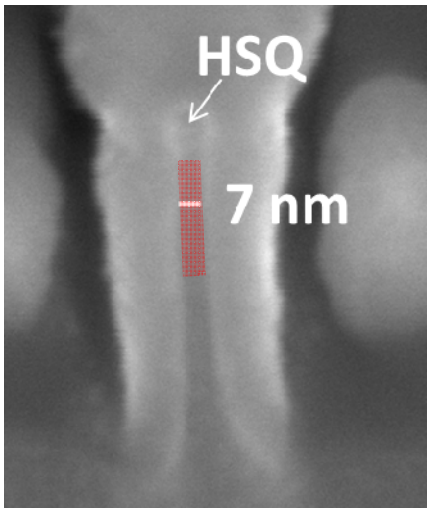




- Sputtered W/Mo contact
- CVD SiO_2 hard mask
- Gate lithography
- Gate recess (Dry): SiO_2/W/Mo
- Active area definition
- Gate recess (Wet): Cap etch
- Fin lithography
- Fin etch
- Digital etching
- ALD gate dielectric deposition
- Mo gate sputtering

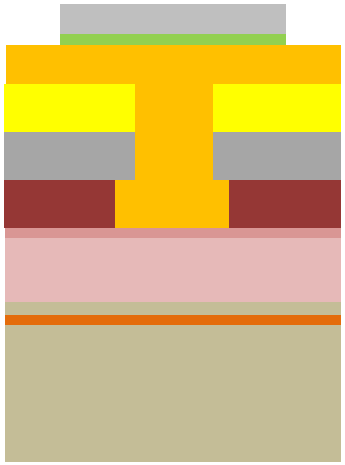


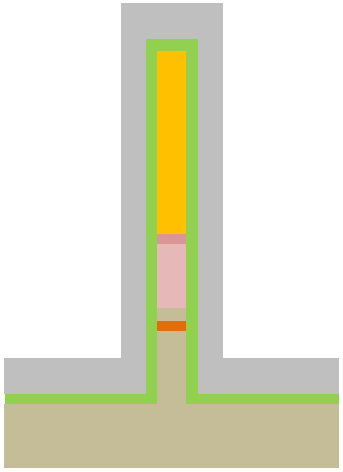


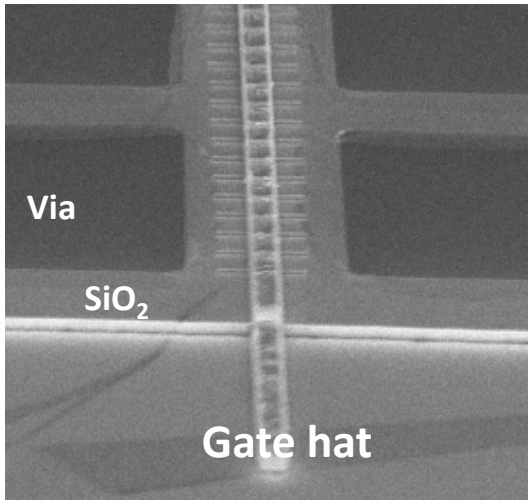


- Double gate FinFET
- HfO_2 , gate oxide EOT = 0.6 nm

Device fabrication



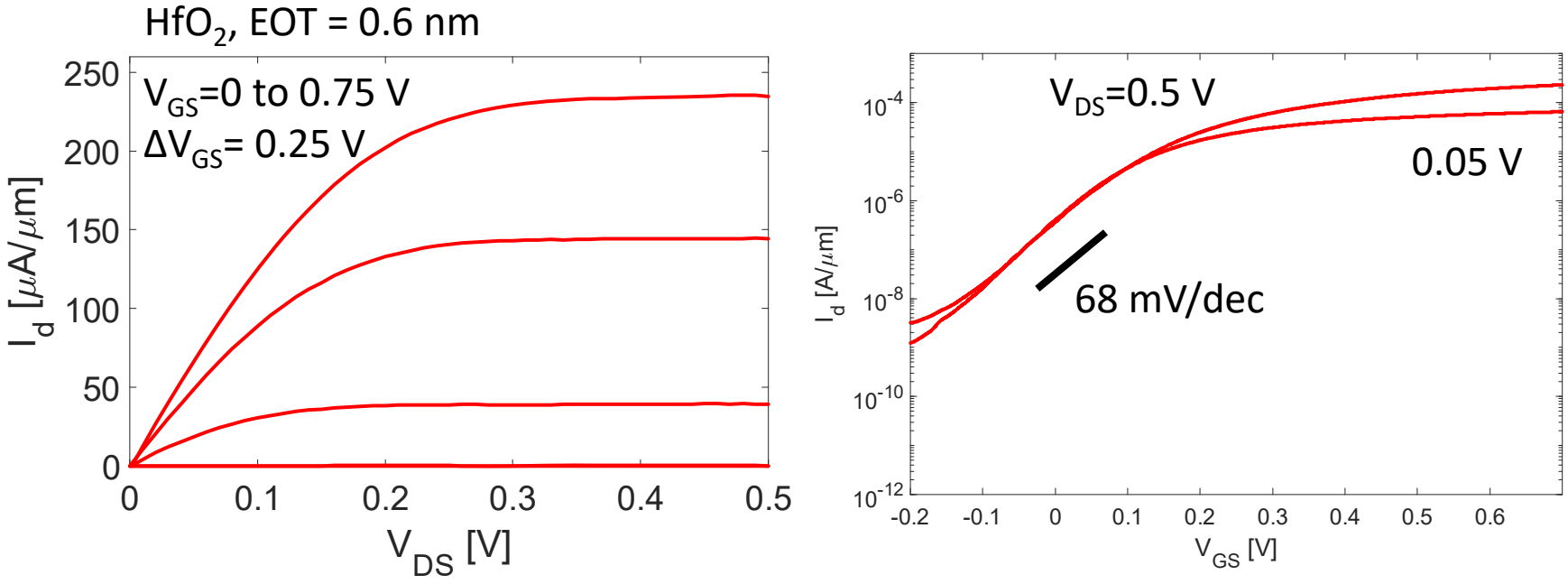




- Fin pitch: 200 nm
- 10-50 fins/device

- Sputtered W/Mo contact
- CVD SiO_2 hard mask
- Gate lithography
- Gate recess (Dry): SiO_2/W/Mo
- Active area definition
- Gate recess (Wet): Cap etch
- Fin Lithography
- Fin etch
- Digital etching
- ALD gate dielectric deposition
- Mo gate sputtering
- Gate head photo and pattern
- ILD1 deposition
- Via opening
- Pad formation

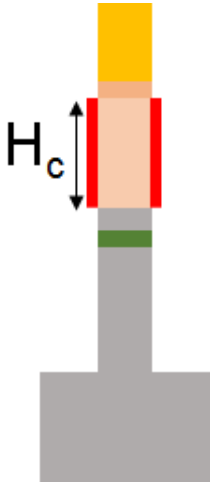
Long-channel characteristics, W_f=22 nm, L_g=0.5 μm

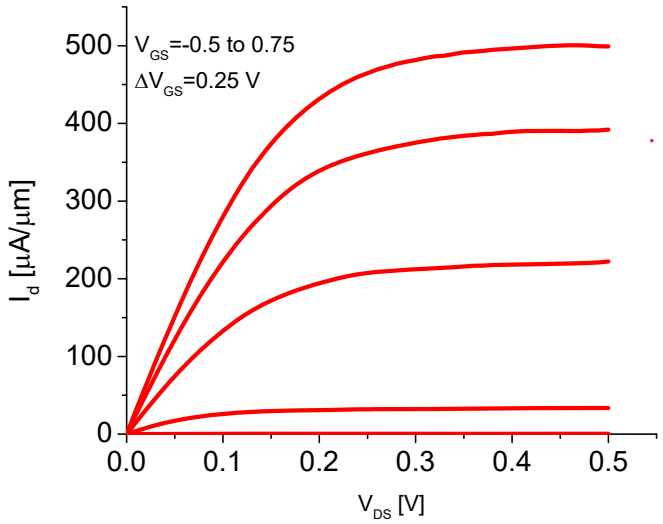


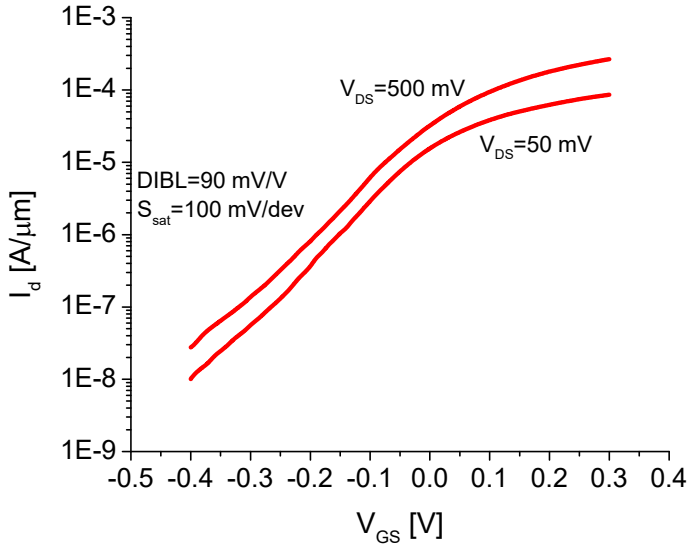
- S_{lin}=68 mV/dec
- Negligible DIBL
- Good electrostatic control over dry etched sidewalls

Most aggressively scaled FinFET

W_f=7 nm, L_g=30 nm, H_c=40 nm (AR=5.7), EOT=0.6 nm:



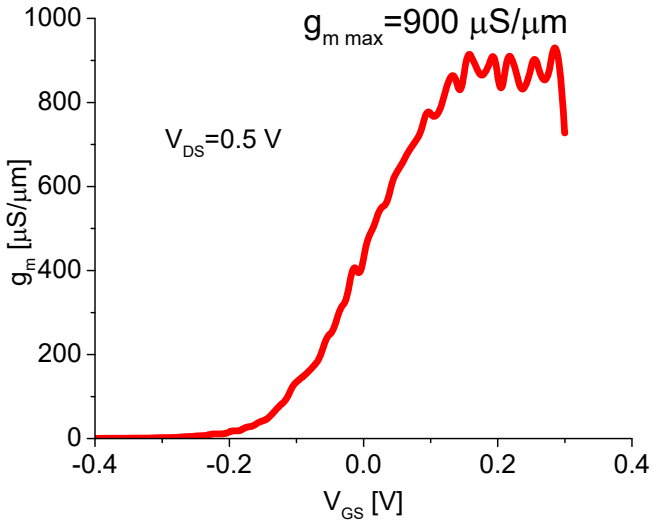




Current normalized by 2xH_c

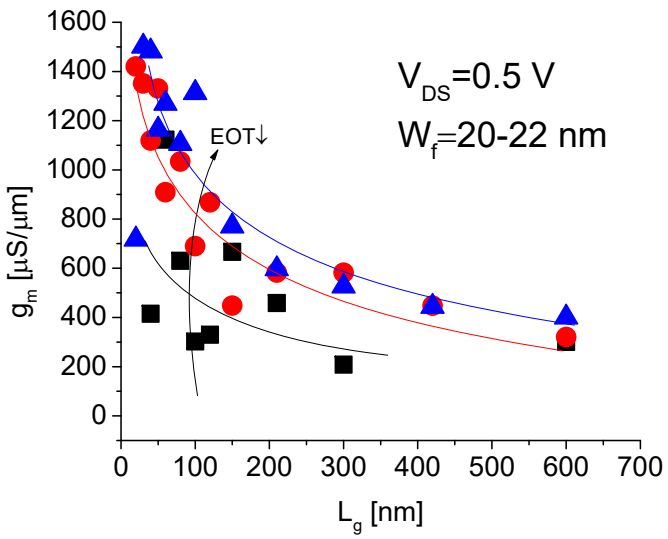
At V_{DS}=0.5 V:

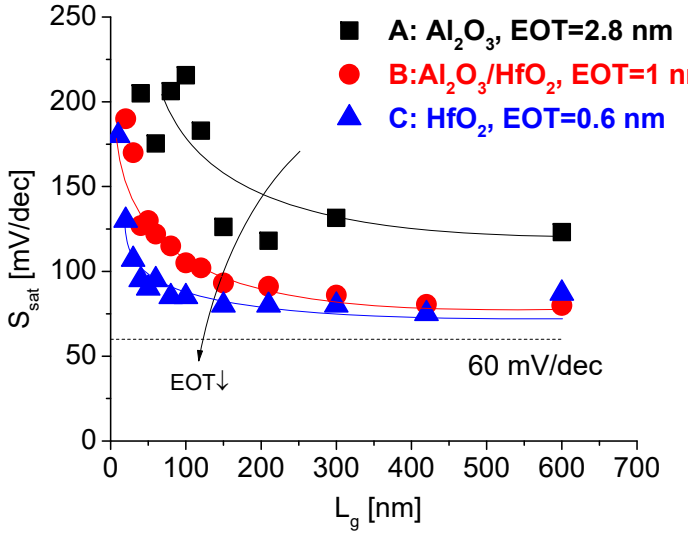
- g_m=900 μS/μm
- R_{on}=320 Ω.μm
- S_{sat}=100 mV/dec

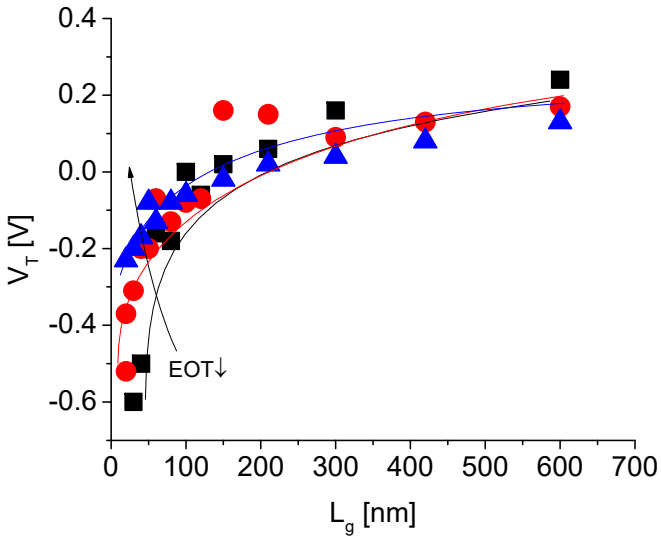


Vardi, EDL 2016

L_g and EOT scaling (W_f~20 nm)



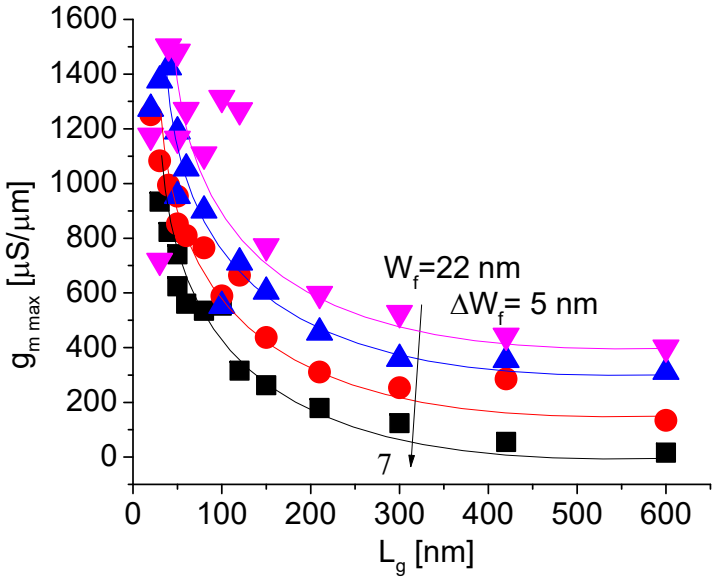


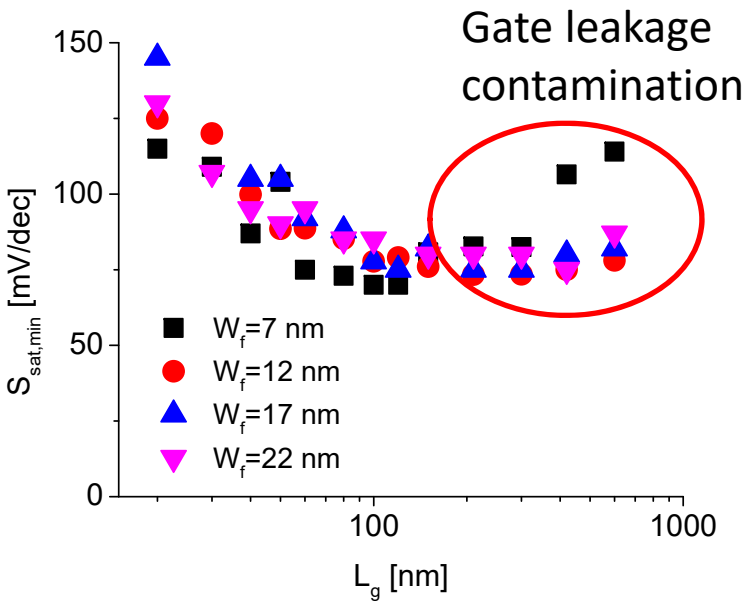


EOT ↓ → g_m ↑, S_{min} ↓, V_T rolloff ↓

Classical scaling with L_g and EOT

W_f Scaling





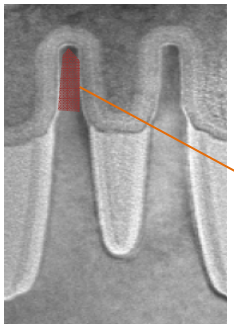
Non-ideal W_f scaling

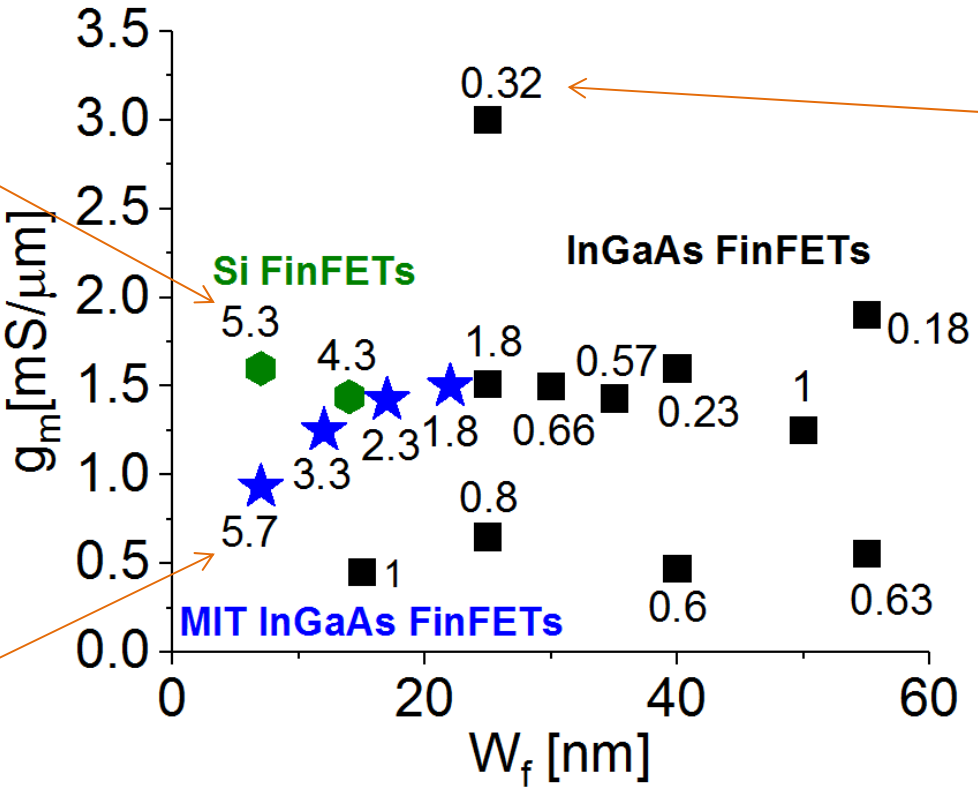
- $W_f \downarrow \rightarrow g_m \downarrow$
- $W_f \downarrow \rightarrow$ Constant S_{min}

- D_{it} (~5×10^{12} $cm^{-2}.eV^{-1}$)
- mobility degradation
- line edge roughness?...

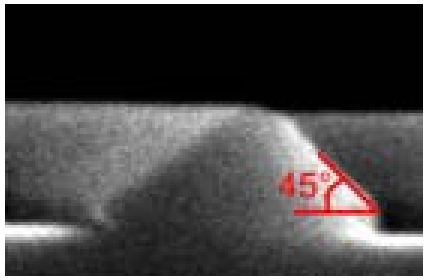
Benchmark

g_m normalized by gate periphery

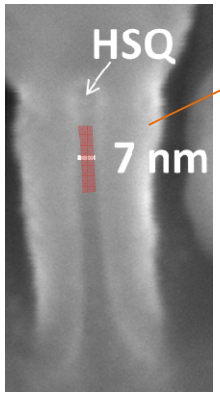


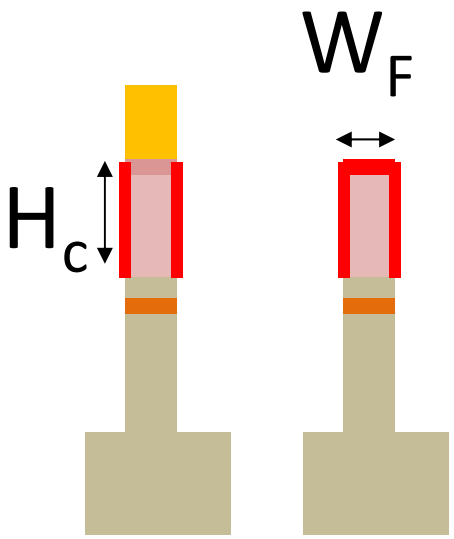


Best logic device both III-V and Si



Zota, IEDM 2016



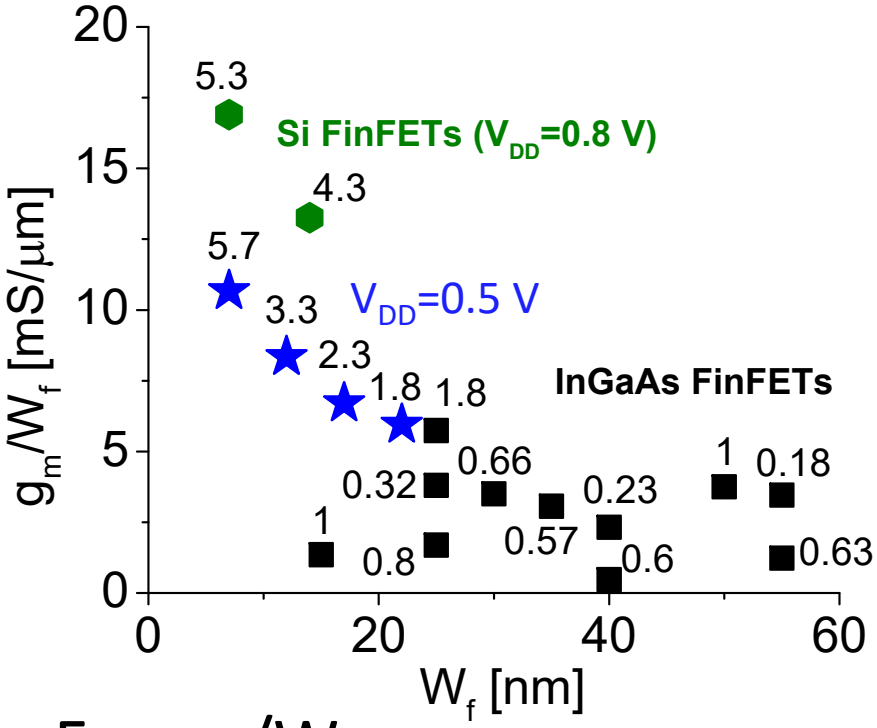


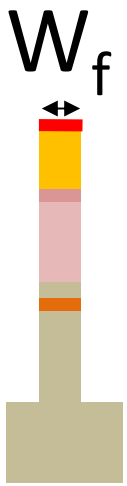
MIT FinFETs:

- AR_c>1
- Sub-10 nm W_f

Benchmark

g_m normalized by fin width

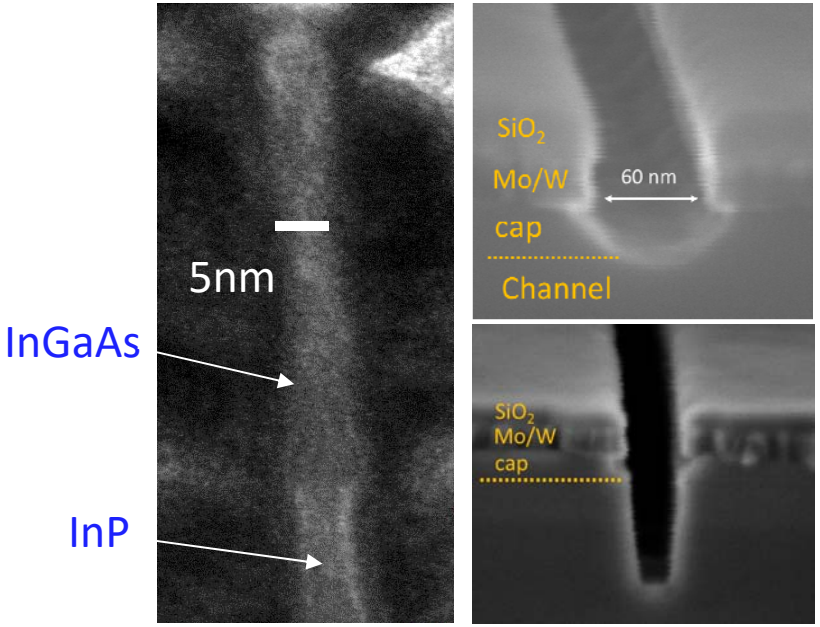


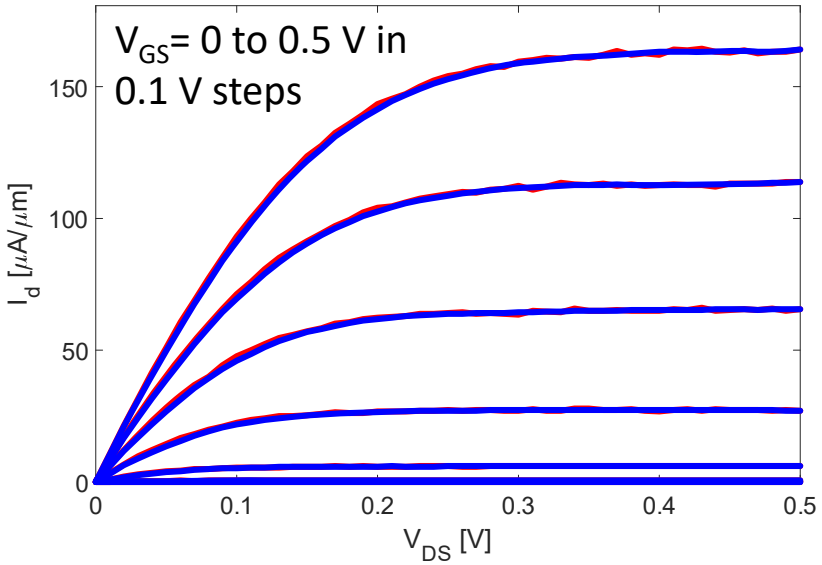


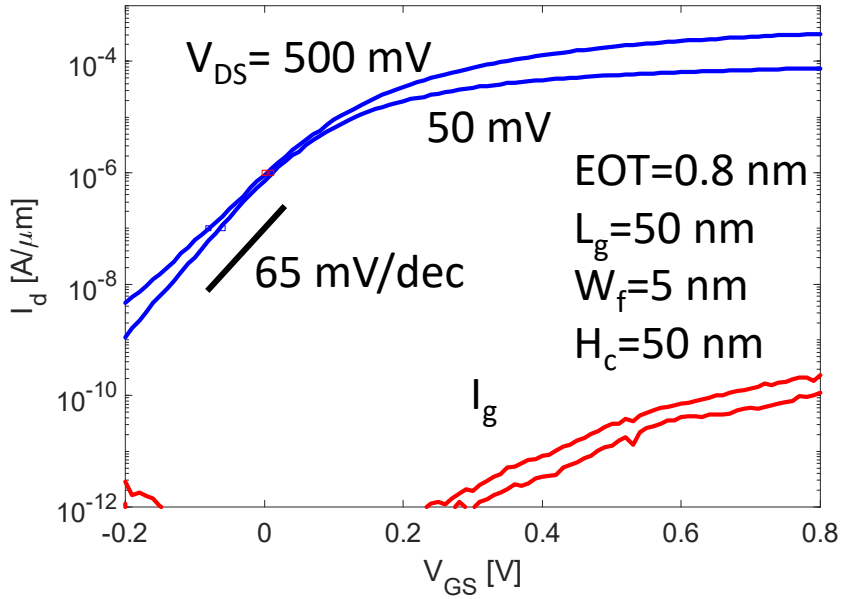
For g_m/W_f:

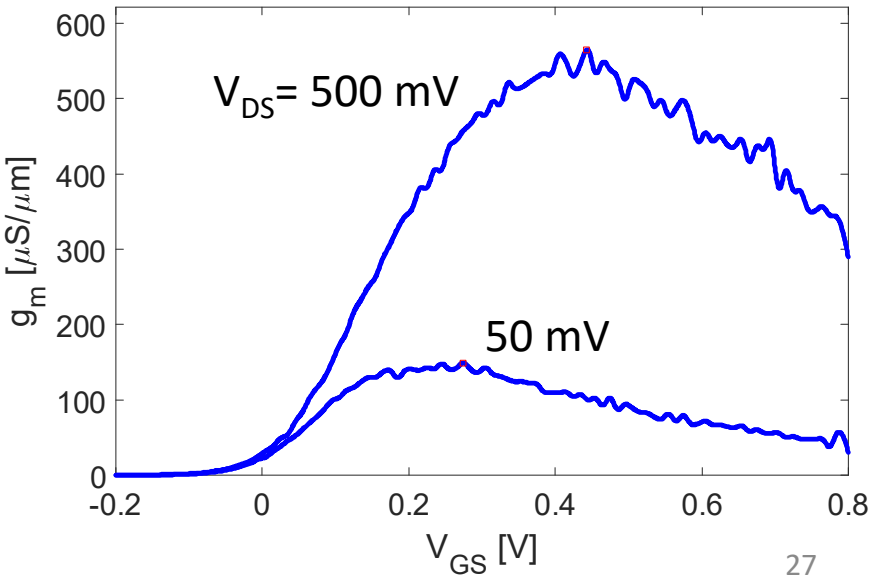
- Si > III-V
- MIT FinFETs > all other III-V FInFETs

Post deadline results

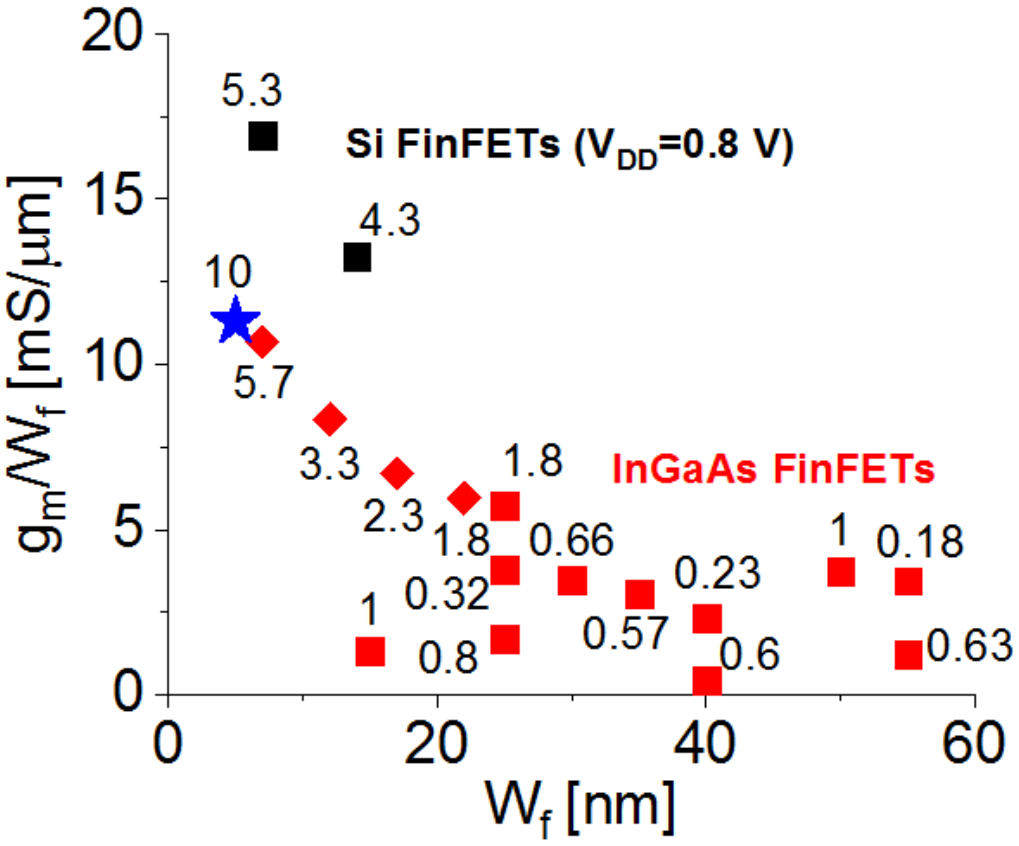








Post deadline results - Benchmark



- Record g_m at W_f=5 nm
- Record AR
- Improved SCE

Conclusions

- Novel self-aligned gate-last FinFET:
  - Self-aligned gate to contact metals
  - CMOS process compatibility
  - Sub-10 nm fin width
  - AR_c>1
  - Double-gate FinFET
- Excellent performance and short-channel effects in devices with L_g=30 nm and W_f=22 nm
- Demonstrated subthreshold swing of 65 mV/dec in short channel devices
- Still short of Si FinFETs performance

Thank you !